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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,923	08/25/2003	Hong-gie Hwang	1293.1884	1952
21171 7590 01/05/2007 STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005		EXAMINER		
		·	FLORES RUIZ, DELMA R	
			ART UNIT	PAPER NUMBER
WINDIII			2828	
SHORTENED STATUTORY	PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE	
3 MONTHS		01/05/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)	
	10/646,923	HWANG, HONG-GIE	
Office Action Summary	Examiner	Art Unit	
	Delma R. Flores Ruiz	2828	
The MAILING DATE of this communi	cation appears on the cover sheet w	th the correspondence address	
Period for Reply	•		
A SHORTENED STATUTORY PERIOD FO WHICHEVER IS LONGER, FROM THE MA  - Extensions of time may be available under the provisions of after SIX (6) MONTHS from the mailing date of this commodified in the second of the	AILING DATE OF THIS COMMUNION of 37 CFR 1.136(a). In no event, however, may a nunication.  Itutory period will apply and will expire SIX (6) MON will, by statute, cause the application to become AE	CATION.  eply be timely filed  ITHS from the mailing date of this communication.  BANDONED (35 U.S.C. § 133).	
Status			
1)⊠ Responsive to communication(s) file	d on 20 September 2006.		
	2b)⊠ This action is non-final.		
3) Since this application is in condition f	<i>'</i> — .	ers, prosecution as to the merits is	
closed in accordance with the practic		•	
Disposition of Claims			
4)⊠ Claim(s) <u>1 and 3-34</u> is/are pending ir	the application		·
4a) Of the above claim(s) is/ar			
5)⊠ Claim(s) <u>18-34</u> is/are allowed.			
6)⊠ Claim(s) <u>1,3-4,7-10</u> is/are rejected.			
7)⊠ Claim(s) <u>5, 6, 11 – 17</u> is/are objected	d to.		
8) Claim(s) are subject to restrict	tion and/or election requirement.		
Application Papers			
9) The specification is objected to by the	Evaminer		
10) The drawing(s) filed on is/are:		by the Examiner.	
Applicant may not request that any object		·	
Replacement drawing sheet(s) including	•		
11) The oath or declaration is objected to	by the Examiner. Note the attached	d Office Action or form PTO-152.	
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim f	for foreign priority under 35 U.S.C. &	5 119(a)-(d) or (f)	
a) ☐ All b) ☐ Some * c) ☐ None of:	ici ici cigir pricing andor co cicici.	110(0) (0)	
· — _ · · · · · · · · · · · · · · · · ·	documents have been received.		
	documents have been received in A	pplication No	
3. Copies of the certified copies of	of the priority documents have been	received in this National Stage	
application from the Internation	nal Bureau (PCT Rule 17.2(a)).		
* See the attached detailed Office action	n for a list of the certified copies not	received.	
Attachment(s)	_		
1) ⊠ Notice of References Cited (PTO-892) 2) ☑ Notice of Draftsperson's Patent Drawing Review (P`		Summary (PTO-413) s)/Mail Date	
3) Information Disclosure Statement(s) (PTO/SB/08)	5) D Notice of I	nformal Patent Application	
Paper No(s)/Mail Date	6)  Other:	<b>⊸</b> ·	

#### **DETAILED ACTION**

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

Claims 1, 3, 7, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Noda et al (6,229,833).

Regarding claim 1, Noda shown Figure 1, discloses a method of automatically controlling an output power of a laser diode (see Fig. 1, Character 11), the method comprising: generating an error voltage between an output voltage of the laser diode sampled during an automatic power control period (see Fig. 1, Character 15) and a reference voltage (see Fig. 1, Character 16a); and performing proportional-integral processing (see Fig. 1, Character 12 and Column 11 Lines 17 – 36) on the error voltage to generate a compensated control voltage (it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does

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not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987)) and applying the compensated control voltage to the laser diode (see Fig. 1, Character 11).

POWER LD 11 14

POWER NONTOR 12 13

ACC ATC

COMPARATOR 160

REFERENCE VOLTAGE 16

LD CURRENT LIMITING CIRCUIT

Regarding claim 3, Noda shown Figure 1, discloses a compensated control voltage applied to the laser diode is an effective control voltage within a predetermined range (see Fig. 1, Character 15).

Regarding claim 7, Noda shown Figure 1, discloses a computer readable medium having embodied thereon a computer program for automatically controlling an output power of a laser diode comprising: generating an error voltage between an output voltage of the laser diode (see Fig. 1, Character 11) sampled during an automatic power control period (see Fig. 1, Character 15) and a reference voltage (see Fig. 1, Character 16a); and performing proportional-integral processing (see Fig. 1,

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Character 12 and Column 11 Lines 17 – 36) on the error voltage to generate a compensated control voltage (it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987)) and applying the compensated control voltage to the laser diode (see Fig. 1, Character 11).

**Regarding claim 9,** Noda shown Figure 1, discloses an apparatus to automatically control an output power of a laser diode, the apparatus comprising: an error voltage generation unit generating an error voltage between an output voltage of the laser diode (see Fig. 1, Character 11) sampled during an automatic power control period (see Fig. 1, Character 15) and a reference voltage (see Fig. 1, Character 16a); and a control voltage generation unit performing proportional-integral processing (see Fig. 1, Character 12 and Column 11, Lines 17 – 36) on the error voltage provided from the error voltage generation unit to generate an effective control voltage (it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987)).

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noda et al (6,229,833) in view of Woodley (2003/0179787 A1).

Regarding claims 4, 8 and 10 Noda shown Figure 1, discloses a method of automatically controlling an output power of a laser diode (see Fig. 1, Character 11), the method comprising: generating an error voltage between an output voltage of the laser diode sampled during an automatic power control period (see Fig. 1, Character 15) and a reference voltage (see Fig. 1, Character 16a); and performing proportional-integral processing (see Fig. 1, Character 12 and Column 11 Lines 17 – 36) on the error voltage to generate a compensated control voltage (it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987)) and applying the compensated control voltage to the laser diode (see Fig. 1, Character 11).

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Regarding claim 4, Noda discloses the claimed invention except for analog to digital converter and digital to analog converter. Woodley teaches providing his device with an analog to digital converter and digital to analog converter However, it is well know in the art to apply the analog to digital converter and digital to analog converter as discloses by Woodley in (see Fig. 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was to apply the well known analog to digital converter and digital to analog converter as suggested by Woodley to the laser of Noda, because could be use the ADC to converter the laser beam to digital signal to the processor can process the information and could be use the DAC to convert the digital signal to the analog signal to can make a feedback in this device to see (see Fig. 3) of Woodley.

## Allowable Subject Matter

Claims 5, 6, 11 – 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 18 – 34 are allowed.

### Response to Arguments

Applicant's arguments with respect to claims 1 and 3 – 34 have been considered but are most in view of the new ground(s) of rejection.

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Delma R. Flores Ruiz whose telephone number is (571) 272-1940. The examiner can normally be reached on M - F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Min Sun Harvey can be reached on (571) -272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

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USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Examiner Art Unit 2828 DRFR/MH

November 20, 2006

Min Sun Harvey Supervisor Patent Examiner

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